Advanced testing using real life evaluation and statistical data analysis

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1 Abstract

Increasing complexity and shrinking lead-time are reducing the time available for system level qualification and reliability testing. These increased time-pressures to qualify materials, processes, PWB vendors and/or products are requiring the electronics industry to modify their testing methodologies and apply alternative statistical analysis techniques.

In order to correlate the statistical data with end use environment conditions we first need to understand the realities of the problems: Is it effective to compare two products to the same pass/fail criteria when their end use environment temperatures differ by 50°C? Is it realistic to take accelerated testing data and statistically predict the life expectancy at a given products operating temperature? To answer these questions is the goal of this study.

The ability to extrapolate acceleration factors is determined by gradually increasing the levels of stress in the product, in-conjunction with advanced statistical analysis. This approach enables the ability to: 1) Calculate an acceleration factor that enables us to predicted product life, at the system operating temperature, 2) Accelerate the time to results in-conjunction with statistically improved confidence and accuracy. The goal is to use accelerated temperature cycling to characterize life, allowing the electronics industry to better tailor Pass/Fail criteria to their products, giving them enhanced predictability for reliability in field life.

2 Introduction

The traditional method for reliability testing of Printed Wiring Boards (PWB) has used thermal stress (air-to-air) oven cycling, as the industry standard. However, due to the inherent drawbacks with this test methodology (extended time per cycle/test, limited upper temperature, difficulties with real time resistance monitoring and grouped failed data) the test method selected for this study was Interconnect Stress Testing (IST).

The IST Technology is available from PWB Interconnect Solutions Inc. This technology uses a test vehicle (coupon) which consists of two independent circuits. The first, "Sense Circuit", is constructed to measure the reliability of Plated through holes (PTH) barrel, this interconnect was the primary structure evaluated in this study. The second, "Power Circuit", consists of internal interconnections between the copper foils and the PTH barrels. The power circuit is also used to homogenously heat the coupon from the inside out, by passing DC current through specifically designed circuits, which match the heating conditions created during component assembly and product operation much more accurately than air to air heating methods.

Throughout IST testing both circuits are continually monitored until a preset level of electrical degradation (structural damage) is achieved, at which point the temperature cycling for each individual coupon is suspended. More Information on the IST test methodology and principles can be found at www.pwbcorp.com

The overall approach used certain thermal conditions to determine an Acceleration factors the primary factors were two-fold. First, the coupons were preconditioned, which is a process used to simulate surface mount assembly and potential rework procedures. In this process a current is calculated and when applied to the test vehicle produces a thermal cycle of 3 minutes to a given temperature. For this experiment the coupons were preconditioned to 230°C, this was repeated for 6 cycles. Second, the coupons were IST cycled at various elevated temperature levels, until structural failure occurred.

All of the IST coupons in this study exhibit a high aspect ratio and were constructed from a high glass transition (Tg) aromatic pheonolic cured non-dicyandiamide base material.

2.1 Coupon Descriptions

All coupons in this study were constructed with a standard IST coupon design file, laminated with 28 layers, which measured 3.8mm (.155") thick. The following table (1) gives a brief description of the design variables tested.

Table: 1

Coupon Identification #	Drilled Hole Size	Pitch / Grid Size	Aspect Ratio
35/66	.35mm/.66 mm (0138" & .026")	1.5 mm (.060")	11 to 1 6 to 1
30	.30 mm (.012")	1.0 mm (.040")	12 to 1
35	.35mm (.0138")	1.0 mm (.040")	11 to 1
45	.45mm (.0177")	1.0 mm (.040")	9 to 1

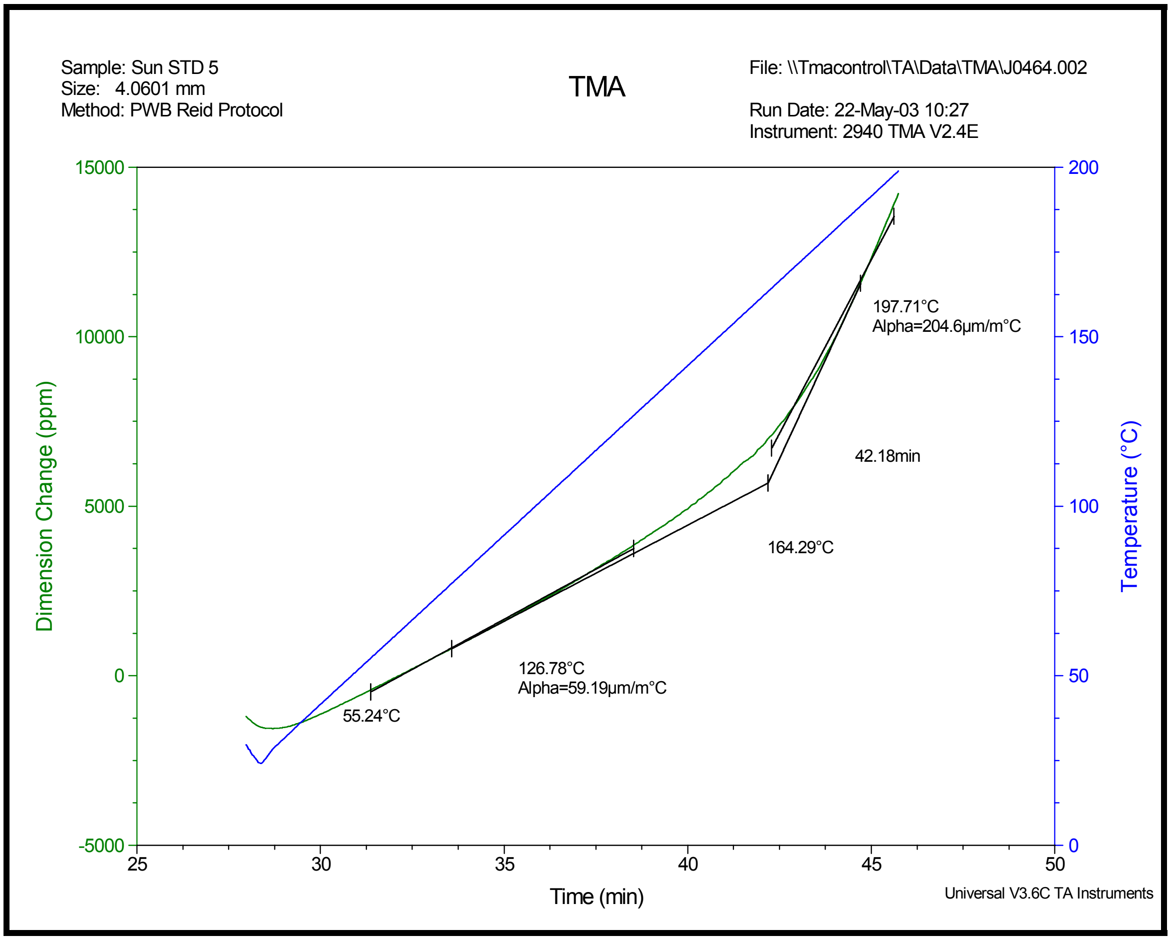
The PWB coupons were fabricated in panel form by one of Sun Microsystems's approved supplier facilities. Each test panel has a total of 24 IST coupons, 6 for each of the 4 designs. The laminate material used was a dicyandiamide (dicy) free, Novolac based epoxy/glass. TG was verified, post build, using TMA (Thermal Mechanical Analysis) to be 165°C and with DMA (Thermal Mechanical Analysis) to be 187°C. All coupons were electrolytic tin plating over copper Metallization. Other Material properties of interest are listed in the following table (2).

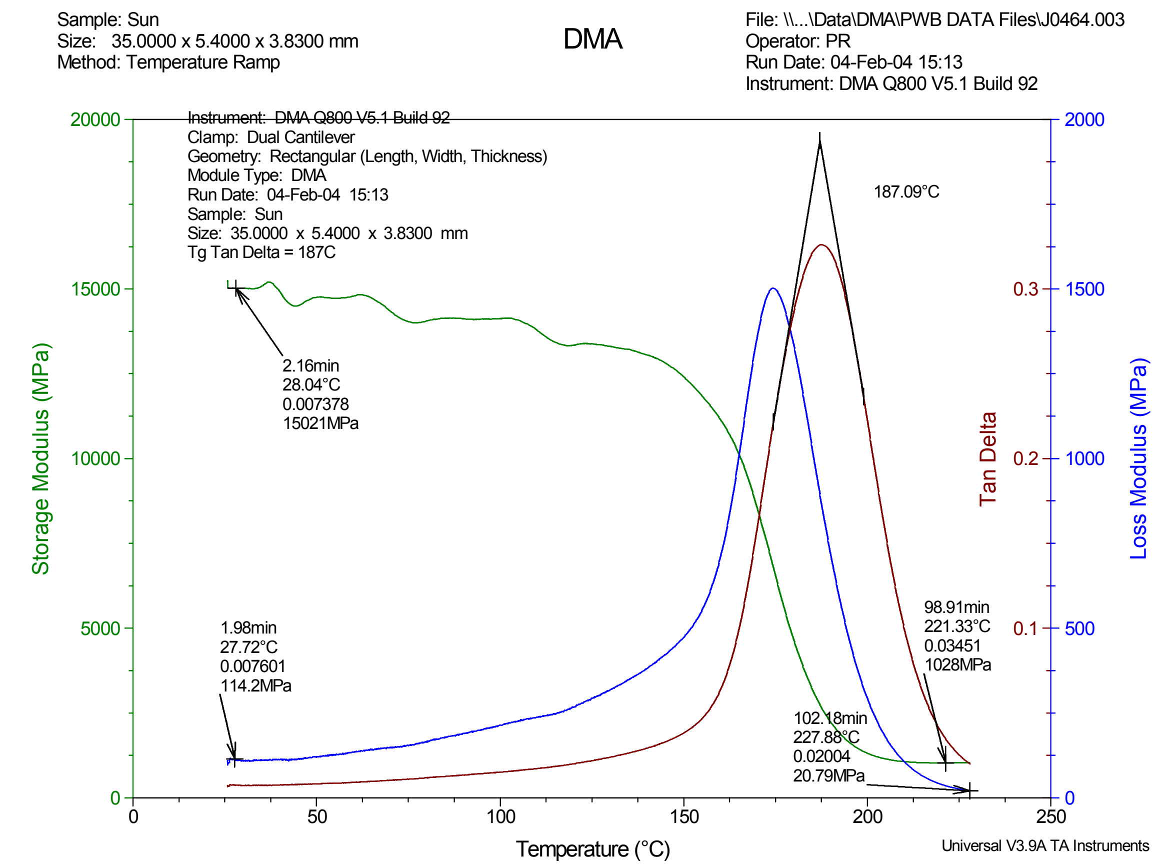
Material Properties

Table: 2

Property	Measured Value	Units
Tg (TMA)	165	°C
Tg (DMA)	187	°C
αCTE	60	PPM/°C
βCTE	198	PPM/°C
α Storage Modulus	15020	MPa
β Storage Modulus	1030	MPa
α Loss Modulus	114	MPa
β Loss Modulus	20	MPa

α = Measured before Tg
β = Measured after Tg


Sample: Sun STD 5
Size: 4.0601 mm
Method: PWB Reid Protocol
TMA
File: \\Tmacontrol\TA\Data\TMA\J0464.002
Run Date: 22-May-03 10:27
Instrument: 2940 TMA V2.4E
Dimension Change (ppm)
Temperature (°C)
Time (min)
197.71°C
Alpha=204.6µm/m°C
42.18min
164.29°C
126.78°C
Alpha=59.19µm/m°C
55.24°C
Universal V3.6C TA Instruments



2.2 Test description

All test completed followed IPC-TM-650, # 2.6.26, "DC Current Induced Thermal Cycling Test". The testing protocol required that all coupons were cycled 6 times from ambient to 230°C, in 3 minutes. This preconditioning step is performed to simulate assembly and rework.

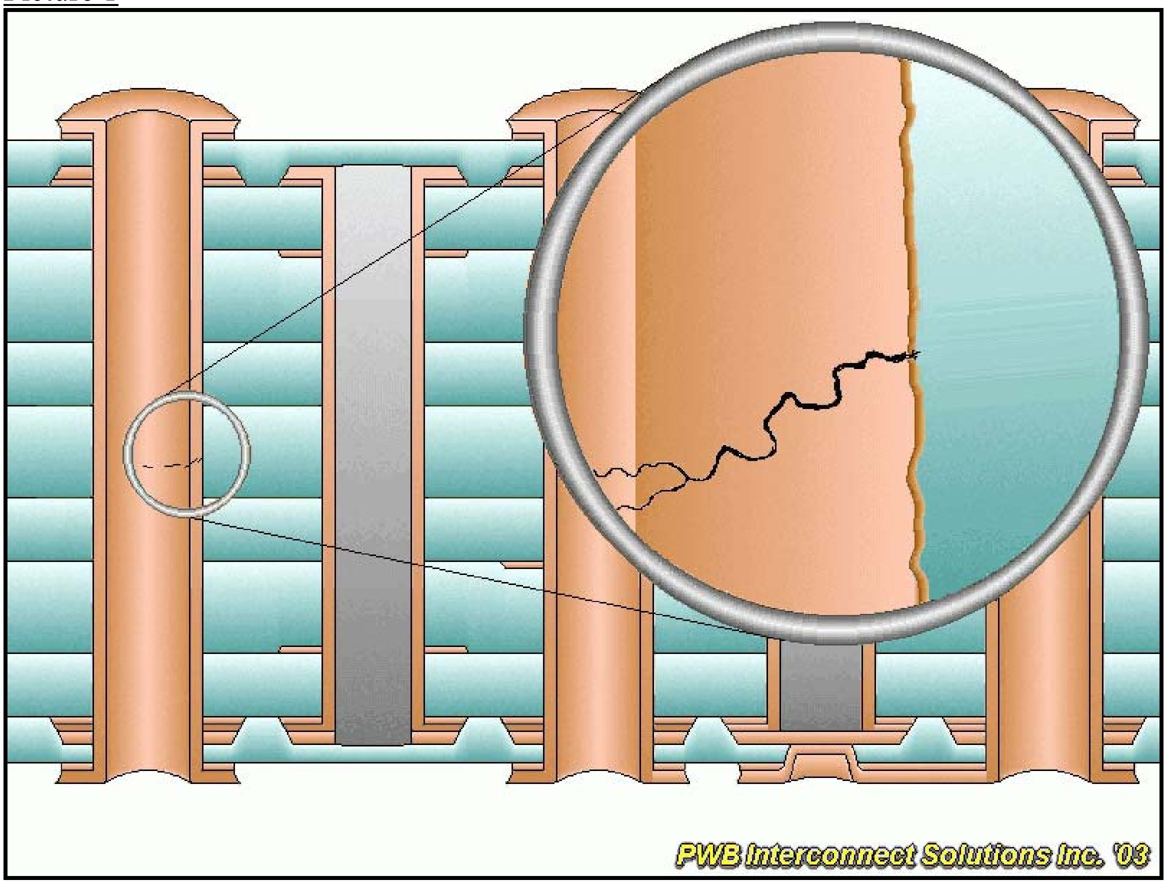
Each design type was randomly grouped into one of three test sets. The three test conditions consisted of temperature cycling from ambient to 130°C, 150°C and 170°C. These test temperatures were selected to give a range near or below the material Tg. For this study one of the objectives was to keep a constant/similar thermal coefficient of expansion (TCE) thereby simplifying the temperature Vs strain relationship.

The IST testing protocol is automated; the only variable changed was the maximum test temperature for each specific test group. The failure criterion, for the power and sense circuits was set at a 10% increase in resistance throughout the entire test and during each individual temperature cycle. Further information on IST testing can be found at www.pwbcorp.com.

2.3 Analysis Methods

The distribution used to analyze the data was a two parameter Weibull. The Weibull distribution is one of the most commonly used and accepted distributions in the field of reliability engineering. Weibull distribution is known as a "lifetime distribution" because of its ability to describe failure characteristics that follow the bathtub curve (infant mortality, useful life and wear out). The region of this relationship that we are interested in, for this study, is wear out, which in the case of a PTH is fatigue failure of the barrel, specifically barrel cracking, refer to picture 1.

Picture 1



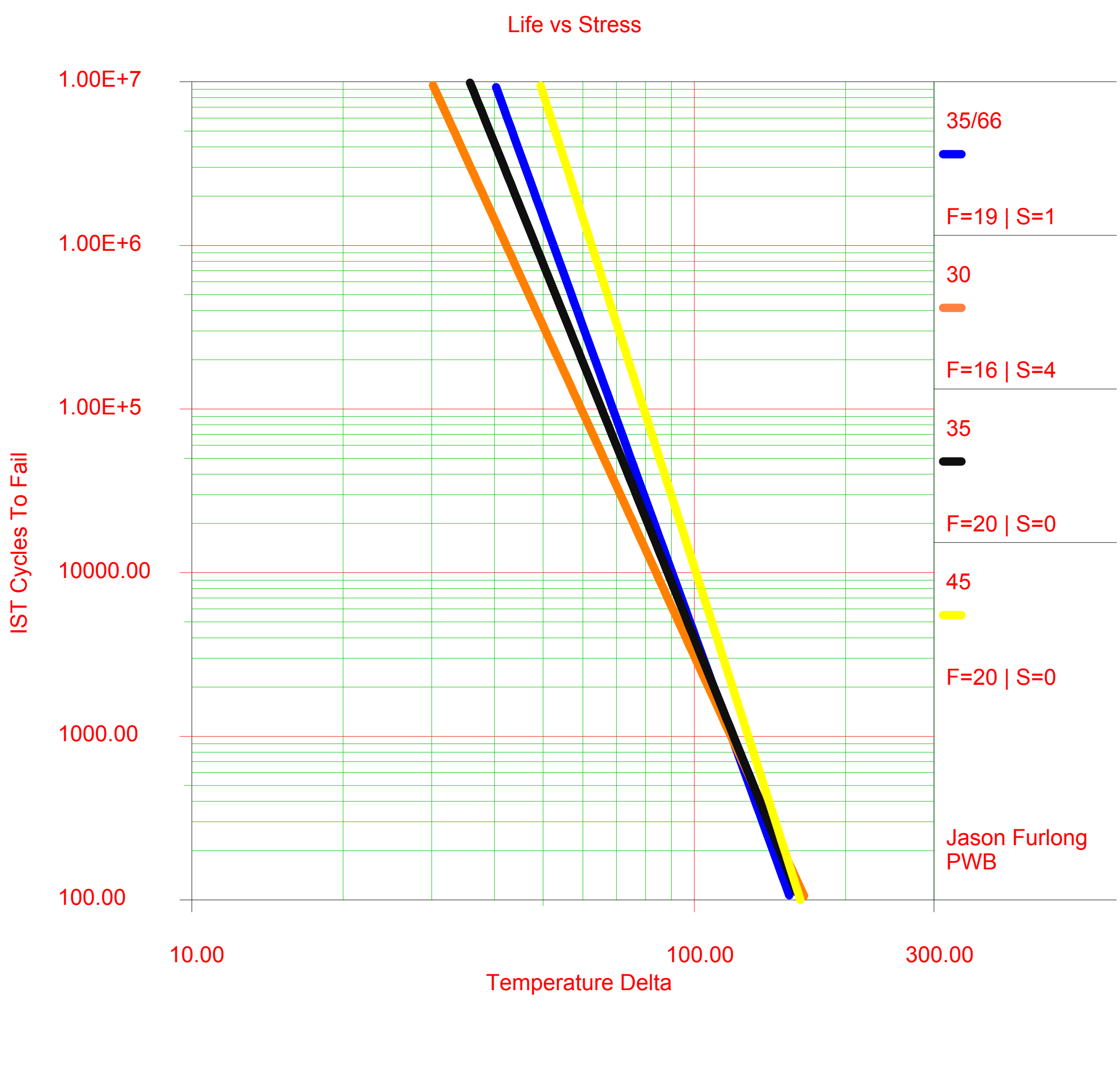
The method chosen for the accelerated life data analysis was an Inverse Power Law Relationship. This model approach was chosen as a best fit to the failure mode experienced with these test vehicles, which was copper fatigue in the PTH barrel. Using this model we want to mathematically relate the results at our three test temperatures, 130°C, 150°C 170°C. Once we have found the accelerated relationship between these three levels of stress we will use this analysis to predict results at other levels of stress.

3.0 Results

All of the following graphs were generated using Inverse Power Law-Stress Relationships, with a Weibull distribution. The Temperature Delta is difference between 23°C and the maximum temperature. The use stress was set to 62°C (85°C peak temp). The Life unit is the number of IST cycles to fail, represented by 10% degradation in the sense side resistance (PTH barrel) for the given coupon. The Sense circuit in these coupons is design to measure the amount of barrel fatigue. The Power circuit is designed to detect Post interconnect separation. In these results there was not a significant amount of damage to the interconnects, all coupons failed for barrel cracks.

3.1 Life vs Stress

Graph 1

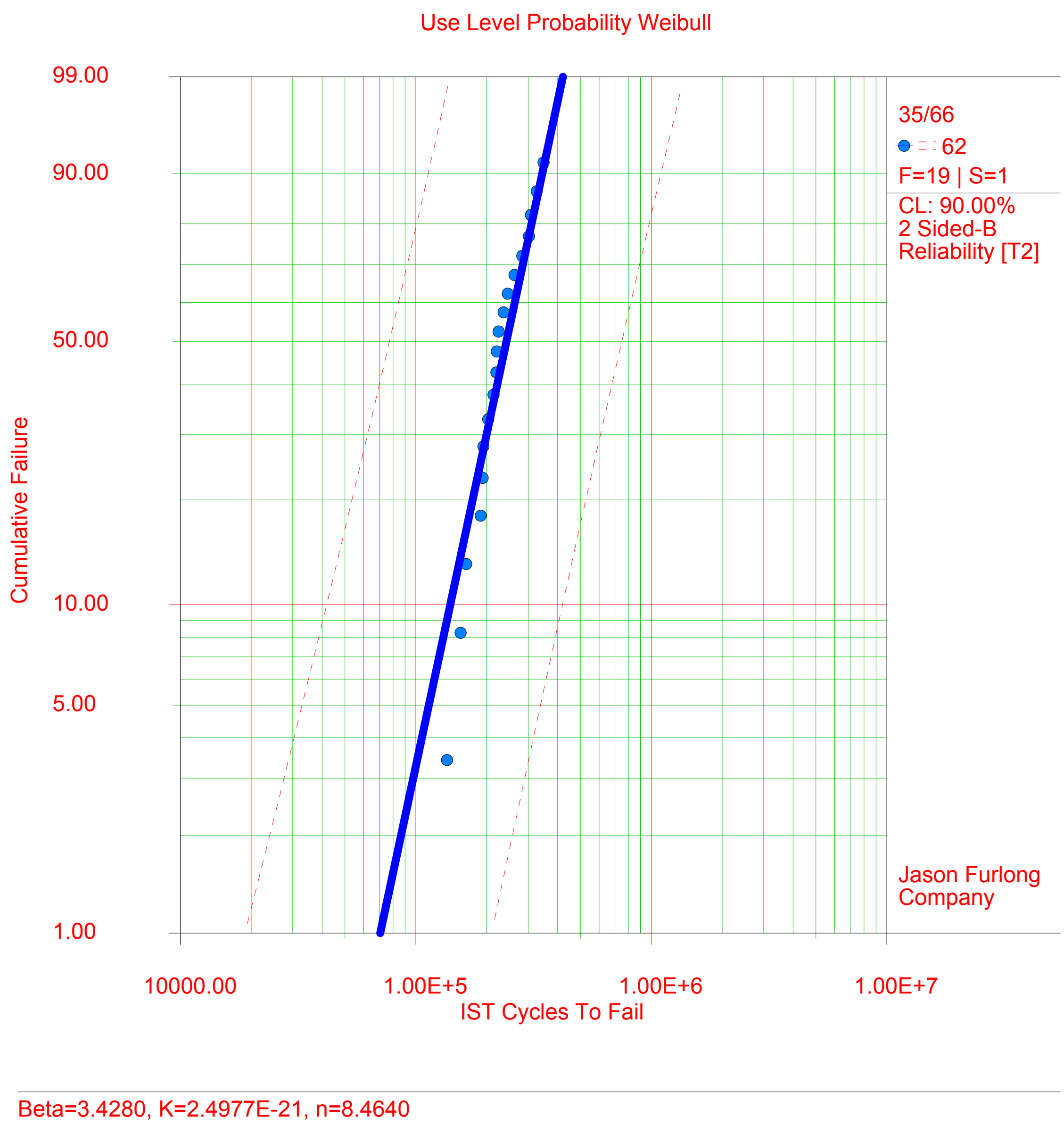


The above Life Vs Stress in graph 1, show a comparison of all four design configurations. An analysis of the graph shows that the performance order is, from best to worst, coupon 45, 35/66, 35 and 30. This result follows both aspect ratio and the pitch size, in an expected manner. However we also see that at high stress levels, about 130 (~150°C) the data starts to converge for these samples, emphasizing the need for acceleration factor analyses.

3.2 Weibull plots for the use stress

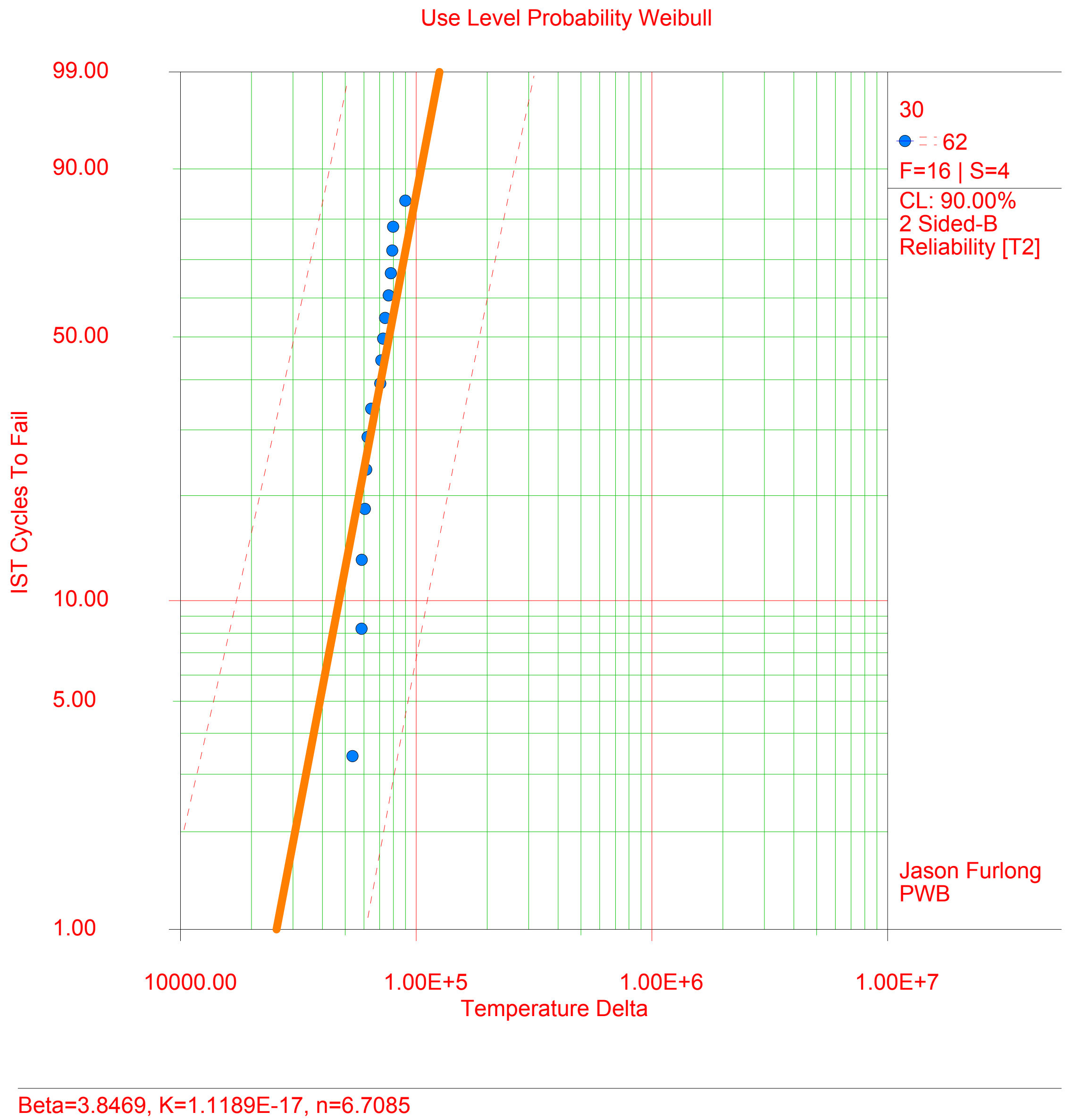
The following four graphs represent the predicted results for each design at there use temperature of 62 (85C peak temp) with a 90% confidence bound.

<u>Graph 2</u>



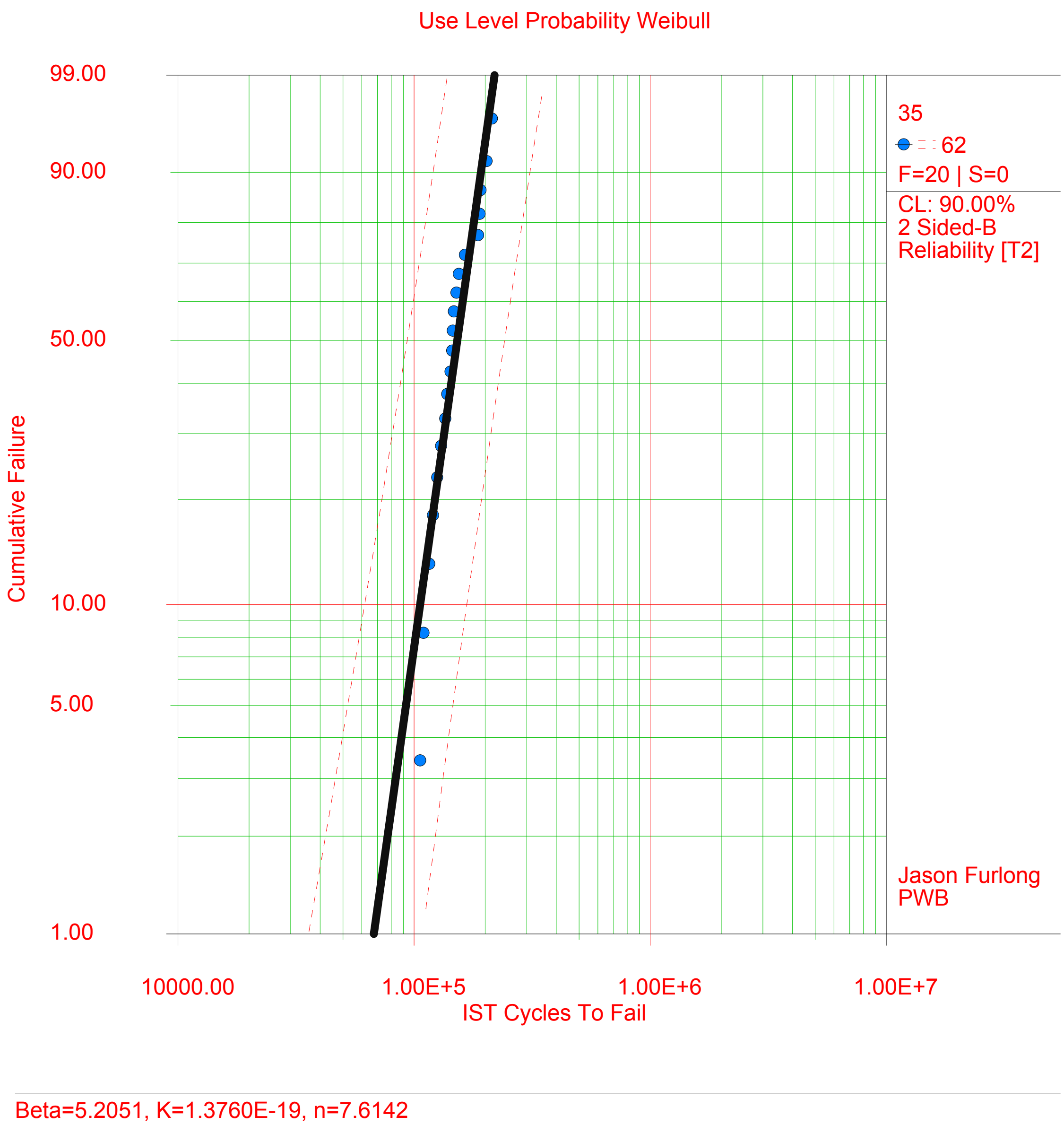
Above are the predicted Stress Vs Life Graphs for the coupon 35/66.

Graph 3



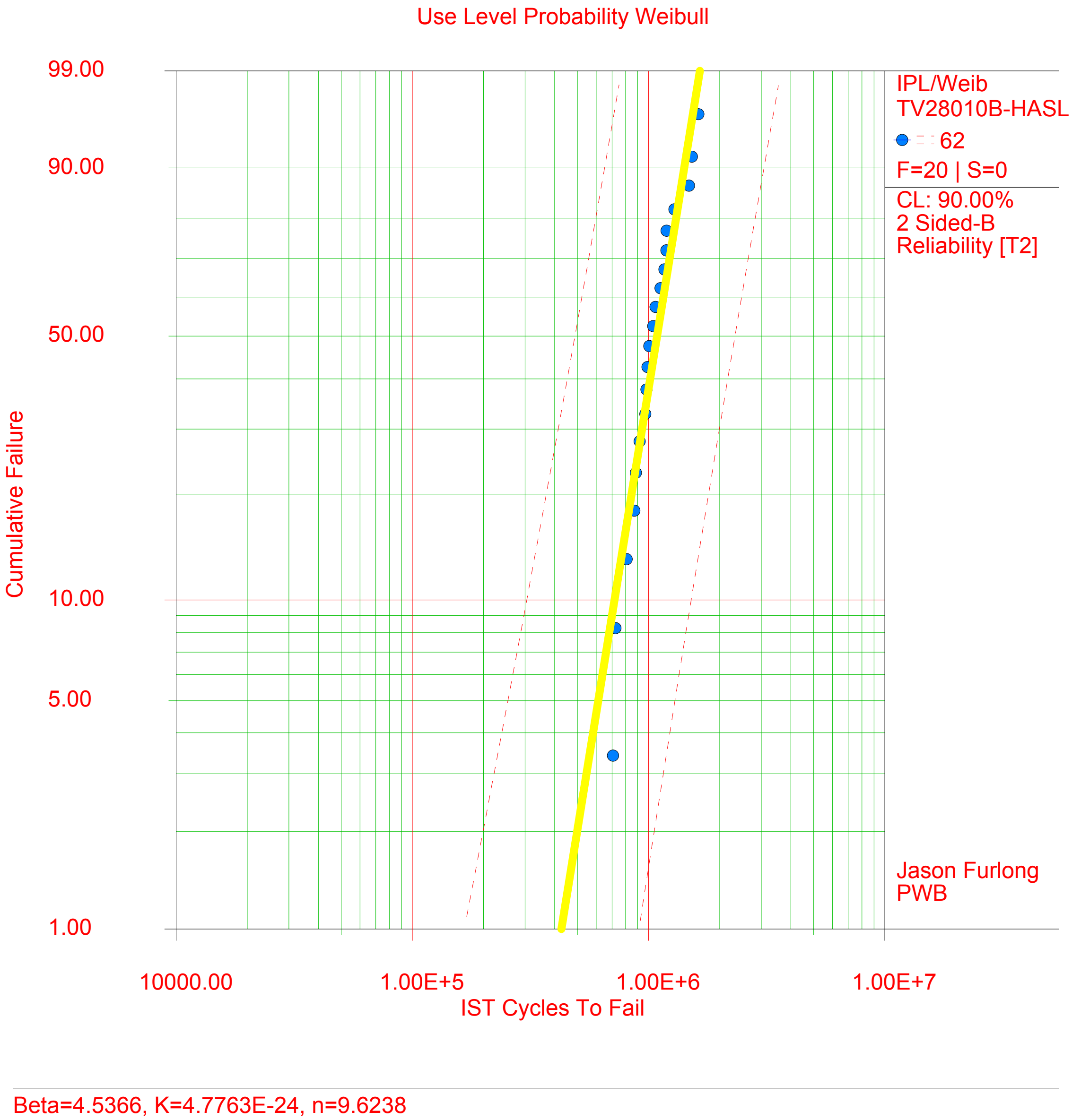
Above are the predicted Stress Vs Life Graphs for the coupon 30.

<u>Graph 4</u>



Above are the predicted Stress Vs Life Graphs for the coupon 35.

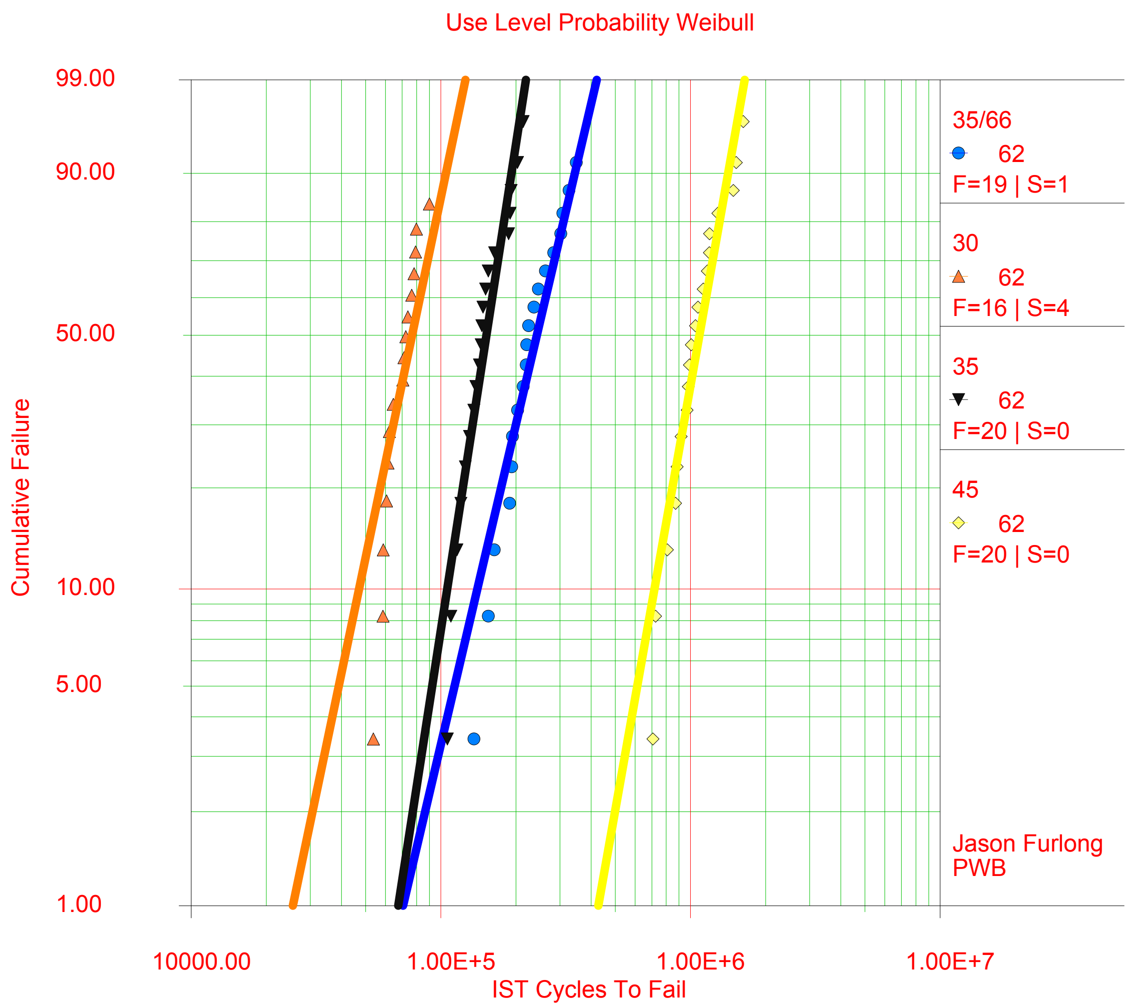
<u>Graph 5</u>



Above are the predicted Stress Vs Life Graphs for the coupon 45.

The following is the predicted results for all designs plotted together.

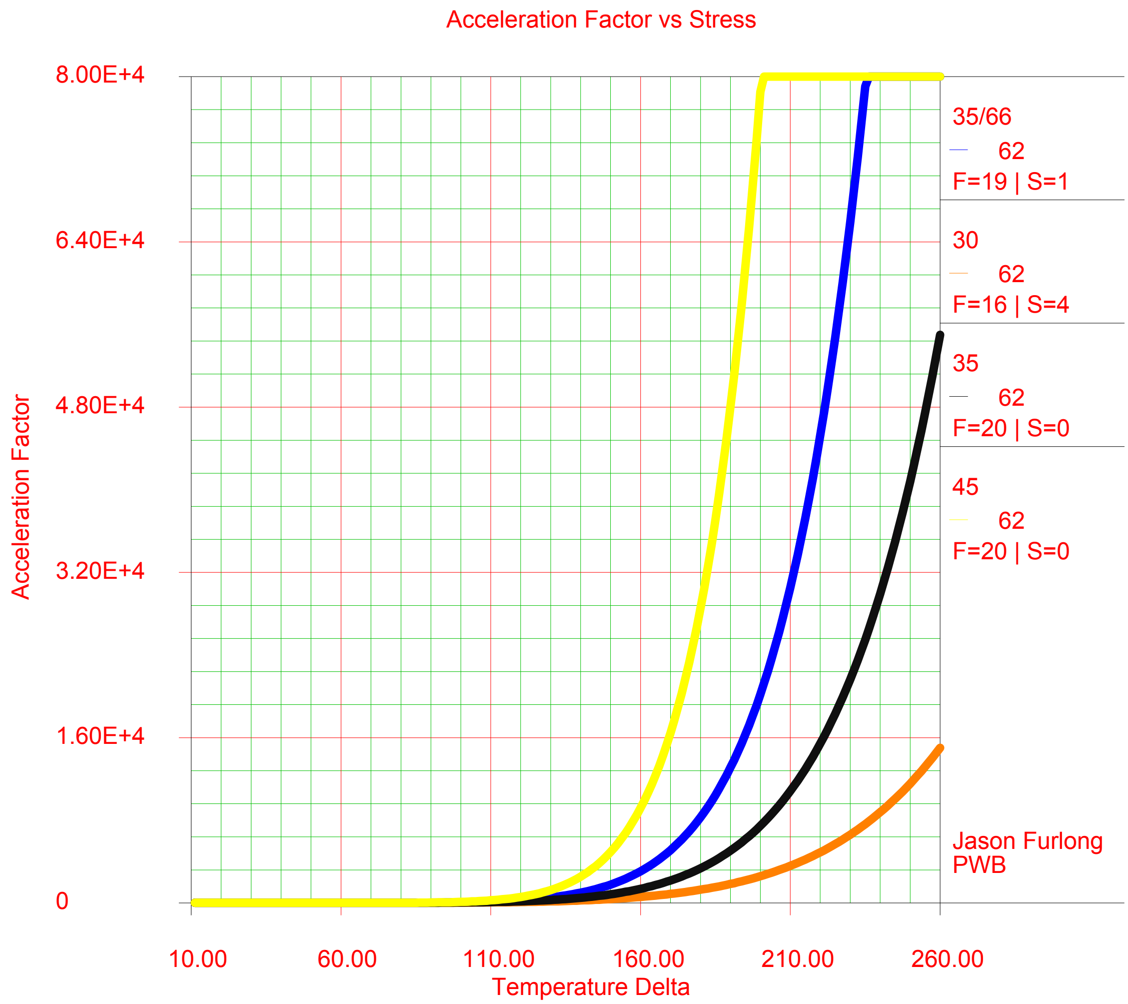
<u>Graph 6</u>



Again A visual analysis of the graph shows that the performance order is, from best to worst, coupon 45, 35/66, 35, 30. This result also follows both aspect ratio and the pitch size, in an expected manner. As can also be seen the data points are a good fit to the line of fit.

3.3 Acceleration factors

Graph 7



The above graph shows a visual representation of the calculated Acceleration factors. The acceleration factors are a ratio between the use temperature and the accelerated test temperature. The use of this acceleration factor method gives us the advantage of accelerated test times while still being able to relate the results to a lower test temperature. This lower test temperature could be the field temperature of a product or the test temperature of a historical baseline. The graph is Stress, which is degrees Kelvin, VS Acceleration Factor. From the graph one could analysis data as follows:

If we assume a minimum of 10,000 IST cycles, at a use temperature 85°C, what is our minimum number of cycles at a higher test temperature with these designs?

At 150°C our results are:

Coupon #	Acceleration Factor	Min Cycles at 150 degrees	Time to results
35/66	432	24	2 hrs
30	122	82	7 hrs
35	235	43	4 hrs
45	993	10	1 hr

At 170°C our results are:

Coupon #	Acceleration Factor	Min Cycles at 170 degrees	Time to results
35/66	1490	7	1 hr
30	327	31	3 hrs
35	715	14	1.5 hrs
45	4056	3	0.5 hrs

4 Conclusions

With this technique we achieve faster time-to-fail results. The faster results could be used to either reduce lead times or increase sample sizes. Increased sample size will lead to more statically valid results and predictions.

Once the acceleration analysis is complete for a given produce we could model its performance at different temperatures. This model could be used to predict the influence of temperature on field life and how a change of use temperature would in turn affect field life.

The analysis could also be used to calculate the use temperature that must be achieved to result in a given reliability.

The results of the type of analysis will lead enable us to set more precise pass/fail criteria when using The IST Technology.

5 Future Works

Investigate most the analysis of acceleration will be effected by testing above Tg to predict a result below Tg.

Use acceleration analysis to determine more precise customer/product specific pass/fail criteria for The IST Technology.

Study the impact of assembly and rework on the life of a coupon.

6 Acknowledgements

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7 References

(1) Jay L. Devore, 1995, “Probability and Statistics for Engineering and the Sciences” Fourth Edition, Brooks/Cole Publishing Company

(2) IPC-Test Manual TM 650, Number 2.6.26, Subject “DC Current Induced Thermal Cycling Test”

(3) “Accelerated Life Testing Reference” at www.weibull.com

(4) “Life Data Analysis Reference” at www.weibull.com