Effects of Lead Free Soldering on "Plating" Vias

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ABSTRACT

The removal of lead from solder and solder pastes to make the manufacturing process of electronic devices more environmentally friendly has created more confusion and uncertainty in the electronics industry than any other single change in decades. The single greatest factor is the higher soldering temperature required for lead free alloys, whether for wave solder, surface mount reflow or rework. Higher temperatures accentuate the mismatch of coefficients of thermal expansion, CTE, between the dielectric material and plated copper, so that higher forces exert greater stress on copper plating, increasing the potential to fail.

This paper will describe the effects of assembly at higher temperatures on materials and processes to produce the plated through vias and microvias. Factors that effect reliability of through vias and microvias will be discussed along with ways reliability can be assessed. Electroless copper plating is challenged to provide adhesion to the new laminate materials. Electroplated copper must keep up with new design requirements, higher aspect ratios, etc. "Difficulty Factor" is a concept used to express the effects of board thickness and via diameter on the plating process. Surface finishes, such as ENIG and Lead Free HASL, can have a positive effect on reliability because they participate in the formation of the solder joint.

INTRODUCTION

Lead free alloys for soldering applications are available in a variety of compositions. The common alternatives under consideration today share the characteristic of higher melting points than eutectic tin-lead, the previous industry standard. Table 1 contains a listing of the alloys most widely studied and their respective melting points. Because of the similarity of its properties to eutectic tin-lead, tin-silver-copper alloys, commonly referred to as SAC, have received the greatest amount of attention and are successfully being used in the early stages of implementation of lead free assembly. A quick scan of the melting points verifies that all of the lead free options melt at a higher temperature than 183^{o}C, that of eutectic tin-lead. Eutectic tin-copper + nickel, a newer alloy that is gaining success as an alternative, melts 10^{o}C higher than the SAC alloys. The higher melting points require higher processing temperatures for wave solder machines, reflow ovens and rework stations. The higher temperature has created concern about the reliability of finished products leading to many studies of materials and processes. Connections are made within the board by plating copper from the electroless process to make the dielectric material conductive followed by electroplating copper to produce the desired thickness. As materials are heated to higher temperatures, the differences in coefficients of thermal expansion, CTE, between resin and copper become magnified and exert an even greater force from z-axis expansion. In the case of high density interconnects in thicker panels, z-axis expansion was already an issue at tin-lead soldering conditions, making new designs even more vulnerable to failure. Over the years, test methods and equipment have been developed to assess the "tendency to failure" or reliability of a circuit board. Techniques to detect the failure mechanism have become more sophisticated and the equipment more powerful to aid in the development process.

Alloy	M. Pt. (^{o}C)
Sn63Pb37	183
Sn96.5Ag3.5	221
Sn96.5Ag3.0Cu.5	218-219
Sn95.8Ag3.5Cu.7	217-219
Sn95.5Ag3.8Cu.7	217-219
Sn95.2Ag3.8Cu1	217
Sn95.5Ag4Cu.5	217-219
Sn99.3Cu.7	227
Sn99.3Cu.7+Ni	227

Table 1. Lead Free Alloys

RELIABILITY TESTING

Methods in Common Use

A recent publication by Holden [1] presented a brief overview of six test systems that are tools in the development of manufacturing processes to meet the demands of higher soldering temperatures. Each system uses a different approach, but the intent is the same, to gain confidence that products being built will perform in a reliable manner. The six coupon systems described were: Parametric Test System (PTS), Conductor Analysis Technology (CAT), Printed Circuit Quality and Relative Reliability (PCQR^{2}), Highly Accelerated Thermal Shock

(HATS™), Interconnect Stress Test (IST™) and PerfectTest. Work in our laboratories is done with the IST method.

Interconnect Stress Testing (IST)

The Interconnect Stress Test System (IST) from PWB Interconnect Solutions, Inc. measures change in resistance of plated through vias, microvias and internal layer connections as holes are subjected to thermal cycling [2]. The method uses the heat generated by passing DC current through the internal layer connection to the via for three minutes to reach the desired test temperature, followed by turning the current (heat) off for a couple minutes (exact time depends on coupon thickness) while the coupon temperature returns to ambient. The "number of cycles to failure" is used to quantify the results, with the default being a change in resistance of 10% at 150°C. More robust materials and processes will withstand a greater number of thermal cycles before failure, with the default being 250.

Data extracted from baseline curves [3] are shown in Table 2 to demonstrate how the reliability of coupons improved with increased Tg from 145° C to 180° C. The greatest benefit, four-fold improvement, was seen in coupons with the lowest thickness and the most severe preconditioning process, 6X @230° C. The data further indicated that reliability, the number of cycles to failure, decreased as the board thickness increased from 2.4 mm to 3.8 mm and as the preconditioning process became more severe.

A study was conducted by Andrews, Parry and Reid [4] to correlate the IST method, by use of coupons containing known "marginal" microvias, with results from assembly and rework under lead free soldering conditions. Microvias are more reliable, since they are of shorter length, than plated through vias, so higher preconditioning temperatures are necessary to show failures in a reasonable test time. The first experiment held the preconditioning cycle constant, 5 cycles at 230° C, followed by thermal cycling at different temperatures in separate runs. The data of Table 3 show that cycling at the standard temperature of 150° C produced no failures after 1,000 cycles after preconditioning 5 cycles at 230° C. As the test temperature was increased, the number of cycles to failure decreased dramatically, with 190° C producing failures by the same mechanism seen in assembly, in the desired 400-500 cycle range.

Temperature	Mean IST Cycles to Failure
150° C	1,000
170° C	789
190° C	464
210° C	76
220° C	44

Table 3. Effect of test temperature on "marginal" microvias [4]

At temperatures below 190° C, failures of marginal microvias may not be detected. In coupons tested above 190° C, the expected modes of failure were seen in addition to those from material degradation.

The second experiment tested the effects of lead free assembly and rework by varying the preconditioning temperature followed by thermal cycling at the standard temperature, 150° C, on coupons containing known marginal microvias. The first 6 coupons failed in the first thermal cycle after preconditioning 6X @260° C, suggesting they had lower reliability than the coupons used in the first experiment. A second set of coupons was run.

Precondition	Mean IST Cycles to Failure	Min	Max
As Is	788	375	925
6X @230° C	443	204	925
6X @260° C	4	2	5

Table 4. Effect of preconditioning on "marginal" microvias [4]

The data of Table 4 show that by increasing the preconditioning temperature to 260° C, the number of cycles to failure for "marginal" microvias decreased from 788 to 4, during cycling at 150° C, a dramatic reduction in test time.

To put the first two tests into perspective, a third study was completed with coupons containing known "good" microvias, with the data shown in Table 5.

Precondition	IST Cycles to Failure at 190° C
As Is	1,923 +/- 155
6X 260° C	1,549 +/- 649

Table 5. Cycles to failure of "good" microvias [4]

When the test program was set for 2,000 cycles, the reduction in thermal cycles to failure was approximately 20% after preconditioning with 6 cycles at 260° C. The data verifies that good microvias are capable of passing more than 1,500 cycles in IST, before failing, which is significantly higher than seen with "marginal" microvias. The study provided test methodology for detecting the reliability of microvias.

Table 6 is a summary of the current preconditioning temperatures recommended for tin-lead solder, lead free solder with thin substrates and lead free solder with standard substrate thicknesses [5]. If the purpose of the test is to simulate assembly conditions, 3 preconditioning cycles at the respective temperature, determined by the alloy and

material thickness, are to be used. Six preconditioning cycles at the appropriate temperature simulate the effects of assembly and rework.

	Assembly	Assembly + Rework
Tin-Lead	3 X 230° C	6 X 230° C
Lead Free Thin Substrates	3 X 245° C	6 X 245° C
Lead-Free	3 X 260° C	6 X 260° C

Table 6. Recommended IST preconditioning parameters [5]

Thermal Shock and Cross Section

A common method for assessing the reliability of through vias is to subject coupons to 6 cycles of thermal stress on a solder pot at 288° C followed by cross section and examination of every via under magnification. An example is shown in Photo 1.Experience has generally shown that boards fabricated with materials and processes for lead free assembly will be reliable, if they pass this test. An added degree of confidence will be achieved from coupons that are free of defects after 10 cycles of thermal stress at 288° C. Lead free solder alloys, such as tin-silver-copper may be used in the solder pot, so long as the solder is being used strictly as a heating medium for detecting potential thermal stress defects, such as barrel cracks. The higher rate of copper dissolution exhibited by lead free alloys, compared to tin-lead, has been recognized [6] and losses in thickness of plated copper from vias in the coupons must be ignored.

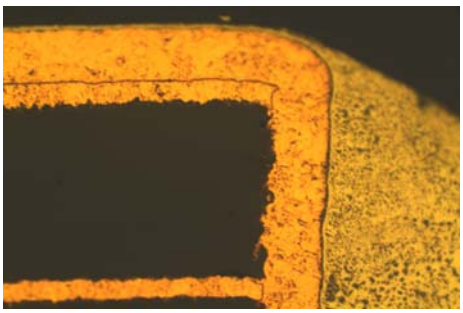

Photo 1. 6X 288° C

LAMINATE MATERIALS

The transition to new laminate materials with greater thermal stability was under way for more complex boards with higher density. The onset of lead free assembly conditions has accelerated the transition and moved the need further down the product complexity scale. Where resin system and Tg were the typical specifications formerly used to characterize laminate materials, new requirements have been developed to define materials with greater stability. Coefficient of thermal expansion, CTE, both below and above the Tg, is now specified. Time to delamination has been extended to more than 30 minutes, when measured by TMA at higher temperatures, 260° C, 288° C or 300° C. Decomposition temperature is measured by TGA where the temperature is increased until the sample loses 5% of its weight. Materials with higher decomposition temperature have greater stability and increase via reliability.

One downside to the use of new laminate materials is that they can be more difficult to process through lines to make vias conductive. Simple adjustments in times, temperatures and concentrations of via preparation process steps may be all that are required. Whenever possible, it is preferred to stay with FR-4 materials to take advantage of their excellent electrical properties and standard processes for metallization.

METALLIZING VIAS

Cleaning and Conditioning Process Prior To Electroless Copper

Through vias are typically drilled while blind microvias are typically laser ablated. Both processes create residues that are left behind and must be removed to provide a robust plated connection. Such residues can be softened, smeared epoxy and debris from drilling as well as residual resin left on capture pads from the ablation process. In either case, incomplete removal of the residues will lead to connections that fail immediately or during thermal testing. An example of a severe microvia failure is shown in Photo 2 and a more subtle failure in Photo 3 [4]. Chemistries to remove these residues from standard FR-4

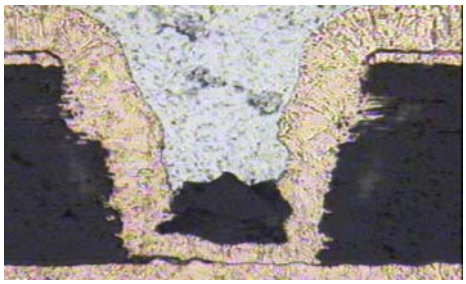

Photo 2. Heavy residue of resin between plating and capture pad

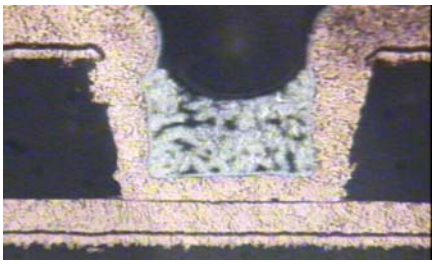

Photo 3. Minor resin residue between plating and capture pad

materials have been in successful use for many years. Typical process parameters are listed in Table 7. When newer, high performance laminate materials are used, identified in the Table as High Tg,

	FR-4		High Tg	
	Temp (^oC)	Time (min.)	Temp (^oC)	Time (min.)
Solvent Swell	70-77	3-6	70-85	5-10
$KMnO_4$ Desmear	70-77	3-6	70-85	5-10

Table 7. Cleaning and Conditioning Parameters

the same solvent swell and potassium permanganate baths typically used for FR-4 can be used, but they usually require higher operating temperatures and longer dwell times to remove the more chemically resistant residues. Solvent swell acts to soften the debris making it more reactive to the oxidative chemistry of the potassium permanganate bath. Water rinses have been omitted from the table.

Electroplating Copper

Factors that affect the reliability of through vias and microvias are thickness, physical properties and uniformity of the plated deposit. When plating microvias, the shape of the microvia is important. Microvias with tapered sides, photo 4 [4], are more easily and uniformly plated with copper and are preferred for that reason over those with straight or re-entrant sides, photo 5 [4].

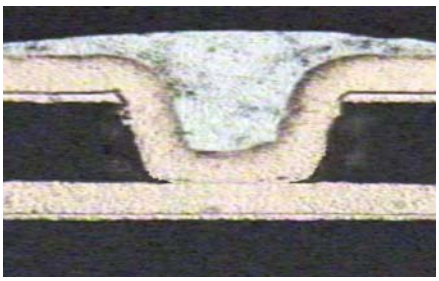

Photo 4. Tapered microvia

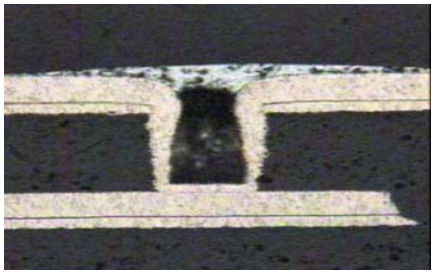

Photo 5. Microvia with straight sides

Thickness of electroplated copper, in through vias and microvias, has a major influence on the continued performance of interconnects. It has recently been stated [7] that with tin-lead solder, copper plating quality is the most important factor determining reliability and with lead free soldering temperatures, material capability joins copper plating for first order influence. Other process steps, such as drilling and board design have a lower order influence. All other manufacturing steps may be optimum, but deposit thicknesses less than 25 microns can cause good product to fail during assembly or during the end use. Measure the copper thickness at the center of the hole, the lowest current density, and be sure it is 25 microns at a minimum.

Deposit properties [8], such as tensile strength and elongation, are easily determined for a plating bath, by plating foils and cutting into strips for testing on a dynamometer, such as the Instron machine, according to IPC-TM-650 2.4.18.1 [9]. Values for elongation above 12% and tensile strength above 248 MPa insure that the deposit has the necessary strength and elasticity to withstand the expansion forces during the multiple thermal cycling stages of assembly and rework, as well as during the end use. Fine-grained, equiaxial deposits with low carbon and sulfur content produce robust vias and microvias. A plating bath with an effective concentration of organic additives is necessary to produce these desirable physical properties. Using the optimum inorganic chemical balance in the plating bath, including copper and sulfuric acid concentrations, also favors increased throwing power for plating at lower current densities without sacrificing the loss in physical properties. This feature is particularly important when plating boards with higher aspect ratios.

The term "difficulty factor" [10] was coined by Rohm and Haas Electronic Materials a number of years ago to quantify the effects of increasing board thickness and smaller via size on plating, by the relationship

Difficulty Factor = Aspect Ratio x Board Thickness = L^2/D

L is the board thickness and D is the diameter of the vias. Since the effect of board thickness is squared, doubling the board thickness from 1.6 mm to 3.2 mm will increase the plating difficulty factor by four, given the same via size.

The effect of reducing via diameter by 50% is to increase the plating difficulty factor by two.

Thickness uniformity of fine features on the board surface and high aspect ratio vias has become more difficult to achieve and remains a challenge. Both direct current, DC, and periodic pulse reverse, PPR, are capable of producing optimum results, depending on design features of the board. Plating with DC at current densities <1.2 ASD works well in a process optimized for low current density plating. For greater productivity, the preferred process is one that deposits the thickest copper at the center of vias for a given production time. PPR processes generally provide higher throwing power at a given current density. As a result, for the most advanced designs, the PPR process has been shown to have greater capability, particularly for product incorporating both through and blind vias.

The benefits of an optimized plating process are realized in continuous production only when used with strict process control. Procedures and methods are not difficult or sophisticated, but they can be minimized or overlooked which, eventually, will lead to problems. With continued neglect, plating defects begin to appear in the boards, such as barrel cracks, for example. Control of the basic bath electrolyte is by wet methods, while additives and by-products from the plating reaction are typically monitored by Hull cell and/or electrochemical analysis. Regular maintenance of the equipment, particularly the filter and anodes, is essential for a consistent plating process. Bath purification by carbon treatment is necessary to remove extraneous organic compounds on a regular schedule, according to the recommendation of the supplier, rather than waiting until defects appear in quality control testing.

Plating Defects

The most common defects in vias which may be attributable to the plating process are barrel cracks, corner cracks, interconnect disconnects (ICDs) and hole wall adhesion. Potential causes are listed in Table 8.

SURFACE FINISHES

A surface finish is used to protect copper pads, traces, vias and interconnects on the bare board while it awaits assembly. This holding time can be from days to months. Some surface finishes, such as Organic Solderability Preservatives (OSP), are very thin and do not participate in formation of the solder joint during wave soldering or reflow of surface mount components. Because of its chemical nature, it also may not withstand the multiple thermal cycles required for mixed technology boards. Others, such as electroless nickel/immersion gold (ENIG), remain on the copper and, at least the nickel, becomes part of the solder joint formed by the attachment of components. It is also capable of withstanding thermal cycles for multi-step assembly.

Benefits and limitations of several noteworthy surface finishes are shown in Table 9, ENIG, electroless nickel/electroless palladium/immersion gold (ENEPIG) and lead free solder from the hot air solder leveling (HASL) process with tin-copper+nickel. One characteristic common to each of the three surface finishes is the role of nickel in providing protection to copper from dissolution in lead free solder alloys.

CONCLUSIONS

Current copper plating technology meets the requirements for soldering with lead free alloys at higher temperatures.

A minimum of 25 microns of copper plated from a properly controlled and maintained plating process will meet the current demands of soldering at higher temperatures.

A brief survey of board fabricators has indicated that 6-10X solder floats at 288^{o} C, the same test and conditions as for tin-lead solder, works well as a test for assessing the quality of through vias and microvias in the field.

New laminate materials with lower CTE insure reliability by reducing the expansion forces along the z-axis of vias.

Preconditioning and test temperatures for IST have been established to adapt the test to lead free soldering conditions.

Surface finishes are available that maintain solderability of the board and facilitate the use of lead free solder alloys.

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Sample Preconditioning	Board Thickness (mm)	Cycles to Failure Tg 145° C	Cycles to Failure Tg 180° C	Calculated Improvement
As Is	2.4	281	979	350 %
As Is	3.2	259	734	280 %
As Is	3.8	223	500	220 %
3X @230° C	2.4	234	905	390 %
3X @230° C	3.2	209	632	300 %
3X @230° C	3.8	168	404	240 %
6X @230° C	2.4	210	843	400 %
6X @230° C	3.2	189	580	310 %
6X@230° C	3.8	134	358	270 %

Table 2. Effect of Increased Tg on IST Cycles to Failure Calculated From Baseline Curves [3]

Fault	Potential Cause
Barrel cracks	Low copper thickness Laminate with high CTE Deposit with low elongation and tensile strength Board design, narrow annular ring which is easier to distort Roughness from poor drilling to produce protuberances leading to thin spots Poor coverage of glass (backlight test)
Corner cracks	"Weak knee" from imbalance of additives to "over level the corner" Laminate with high CTE Brittle copper
Interconnect defects	Poor drilling Excessive smear covering innerlayer connects Inadequate preplate process for electroless copper; chemistry, temperature, time, concentration Back light test is necessary to insure complete hole coverage
Adhesion of hole wall	Poor drilling Excessive smear Solvent swell, permanganate desmear are ineffective

Table 8. Plating Defects and Potential Causes

Surface Finish	Benefits	Limitations
ENIG	Uniform thickness Plating not a thermal cycle Good contact conductivity Thermo-sonic and direct chip assembly Capable of multiple thermal cycles Long shelf life Fine pitch Excellent solderability Capable of electrical test	Not wire-bondable High cost Not easily reworked by fab May influence high signal speeds
ENEPIG	Pd protects the Ni surface Aluminum wire bondable Uniform thickness Fine pitch Plating not a thermal cycle Capable of multiple thermal cycles Long shelf life Excellent solderability Capable of electrical test	Additional process step Higher cost Not easily reworked by fab May influence high signal speeds
LFHASL	Excellent solderability Low cost Ease of application Established process and performance Easily reworked Good bond strength Capable of multiple thermal cycles Capable of electrical test	Variation in thickness; non-planar Counts as a thermal cycle Fine pitch

Table 9. Characteristics of Preferred Surface Finishes