

## **Microvia Reliability**

### **Concerns in the Lead Free Assembly Environment**

**Joint Paper By**

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#### **Abstract**

Traditionally microvias have been considered to be the most reliable interconnect structure within a printed wiring board (PWB). With the advent of lead free assembly, the vulnerability of high density interconnects to fail has increased. This is due to the elevated temperatures experienced during assembly and rework. Over the last 24 months microvias have been found to fail during assembly and in their end use environment. This was noticed in North America and Europe in the spring of 2003. This paper outlines a case study of microvia failure; reliability test methods, failure analysis, fabrication process considerations, and impact of tin/lead and lead free assembly process on microvia reliability.

#### **Background**

Curtiss-Wright experienced opens (and intermittent opens) at electrical testing of their printed circuit boards (PCB) after assembly. Assembly includes double sided surface mount components in addition rework procedures when applicable. Assembly and rework procedures were well defined and tightly

controlled. The opens demonstrated sensitivity to thermal change and mechanical stress. Specifically, connections would become resistive or open under thermal or mechanical stress. Using infrared thermal imaging techniques the defective interconnections were located, subsequent microscopic evaluation demonstrated random failures associated with microvias. The first microvias reviewed demonstrated a target pad to copper plating separation. A small percentage of microvias exhibited barrel cracks, and, on occasion, knee/corner cracks.

These failures were found to be related to specific fabrication date codes and specific vendors. Some of the boards with failing microvia were fabricated by Coretec and were certified compliant to established acceptance criteria. The date codes involved had been tested at PWB Interconnect Solutions and had met the established criteria for acceptance for thermal cycle testing of IST coupons.

This paper is offered as a collaborative effort between Curtiss-Wright, Coretec Inc. and PWB Interconnect Solutions Inc.

## **Test Method**

The reliability test method used throughout this study was Interconnect Stress Testing (IST), as per IPC TM650 – 2.6.26, *DC Current Induced Thermal Cycling Test*. The associated coupons were preconditioned by exposing them to five thermal excursions to 230<sup>0</sup>C, in exactly three minutes. This method of preconditioning was established as the standard for Curtiss-Wright based on a significant volume of data points used in previous testing. This preconditioning method is meant to emulate, but not replicate, three assembly cycles and two rework cycles. IST thermal cycling to 150<sup>0</sup> C was completed on the suspect lot of microvia coupons, the results surpassed the customer's acceptance criteria of a lot mean of 150 cycles, and a minimum of 100 cycles to failure. The suspect lot had achieved a mean of 750 cycles with some coupons achieving a maximum of 1000 cycles (end of test).

In support of IST evaluations, microsections were used to determine the type and cause of failure. The microsection methods used were in accordance to IPC –650 2.1.1 *Microsectioning Manual Method*. Microscopic evaluations of microvia were performed after a mild microetch.

## **Microvia Study - Goals**

A multiple discipline study was initiated by Curtiss-Wright and undertaken to understand the various types, and mechanisms contributing, to microvia failures focusing on:

1. How to prevent reoccurrence of microvia failures.

2. How to improve test methods to identify suspect microvias and accept reliable microvias.

The joint effort between CWCEC (OEM and Assembler), Coretec Inc. (PWB Supplier), and PWB Inc. was established to resolve these microvia reliability concerns.

This investigation included; improvements to metallurgical methods (metrology) necessary to identify and evaluate microvias, analysis of various process parameters required to eliminate the underlying cause of these failures, development of reliability test methodologies to quickly and accurately determining the reliability of microvias and the establishment of criteria for product acceptance or rejection. This study was extended knowing that stress of thermal excursions in a lead free environment would be significantly higher.

### **CWCEC's Concerns and Considerations**

During routine assembly at CWCEC a trend was identified where some PWBs had circuits that were open while other exhibited high resistance. This condition was found during testing and rework on PCBs with a specific date code. The first step was a careful review of the assembly and rework processes for any anomalies in practice or procedure. All processes and process parameters were found to be within acceptable limits. Controls were found to be in place and appropriate. There was no evidence of elevated or prolonged thermal excursions. It was demonstrated that the established assembly and rework procedures did not degrade the integrity of the PWBs.

It was concluded that the established IST testing at 150<sup>0</sup>C did not adequately identify the level of quality on the failing microvias. The coupon from the failing lots had exceeded the established minimum requirements of a mean of 300 and no coupon below 150 IST cycles to failure. The failing lot achieved a mean of 782 cycles with a minimum of 563 cycles to failure; one coupon survived to end of test at 1000 IST cycles.

It was determined that two products were affected: one already partially delivered and another was a "development model". Delivered product was recalled; both produces were scrapped as per procedure.

In response to these developments two parallel actions were launched. CWCEC initiated failure location, micro sectioning of suspect interconnection with failure analysis on a defective PWBs that had been identified as having several sites of opens or higher resistance interconnections. Microsections indicated some microvias with separation of the target pad and the base of the microvia. The second activity was initiated by PWB Interconnect Solutions to determine how this particular defect could be better detected. A proposal was accepted to explore the possibility to use the remaining IST coupons in an Experiment to

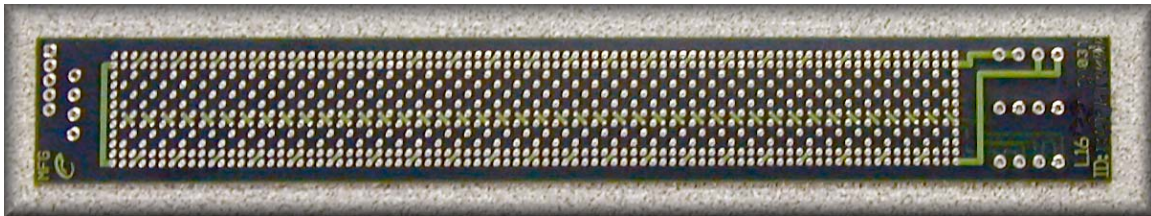
determine what temperatures may be used to improve the detection of defective microvias.

In conjunction with these actions a more robust material was implemented for PWB fabrication that was better suited to withstand the rigors of assembly and rework, and had a lower coefficient of thermal expansion (CTE) which would reduce the strain generated during the thermal excursions associated with assembly and rework.

### **The Physics of the Test Vehicle**

IST coupons are specifically designed to have interconnect structures that are sensitive to increases in resistance. A proprietary method allows the IST coupons be engineered to focus on the robustness of the interconnection of interest. The coupon is also design large enough to contain hundreds of interconnect structures in order to test a statistically significant sample of interconnects. IST Coupons have at least two circuits; a power circuit P1 used to heat the coupon (and test internal interconnections) and a sense circuit S1 for testing the interconnect structure of interest. The coupon used in this study (TV16002) has one power circuit P1 with a PTH interconnect (layers 1/16) and 3 senses circuits where S1 is a PTH (1/16), S2 is a core via (2/15) and S3 is a microvia (1/2 15/16). Each TV16002 coupon contains 340 microvias.

**TV16002B Coupon  
Photo 1**

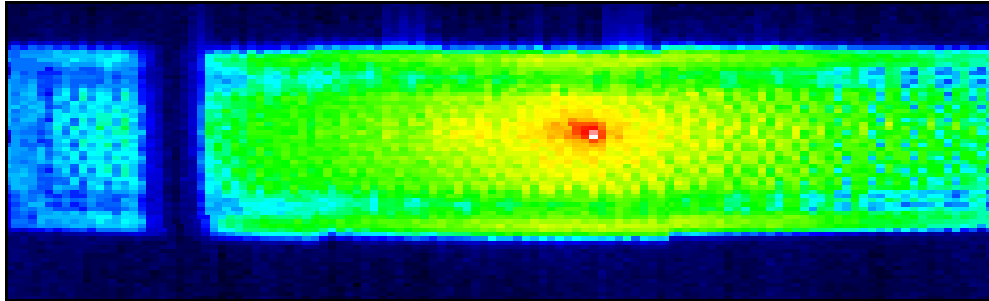


### **Microvia Failure Location**

In an IST evaluation testing automatically stops when a circuit reaches a 10% increase in resistance. The failing coupons have circuits that are still electrically conductive but have a modest increase in resistance. Because the test stopped well before catastrophic failure (open), it is possible to identify the exact microvia that is contributing the highest resistance to the circuit using thermo-graphic techniques. The one worst-case microvia, in a group of 340, may be identified using thermal imaging cameras in a technique called “failure location”. Since the failed circuit has experienced only a 10% increase in resistance, a DC current can be applied causing the failing interconnection to heat. The compromised microvia has a higher resistance, compared to other connecting traces and other (robust) microvias, and it will become the hottest structure in the coupon, and easily found using a thermographic camera. The

thermographic camera allows direct visualization of the exact location of the hottest microvia. The worst case failing microvia is seen as a high temperature hot spot on the surface of the coupon. This is a powerful tool for finding failure locations for subsequent microsection analysis.

**Thermograph of a Failing Via  
Photo 2**



### **Failure Analysis of Microvias**

The established method for evaluating microvias by microscopic technique requires that the microvia to target pad interface to be examined without the use of a microetch. Examining an un-etch cross section of a microvia can be used to good effect in fabrication, however, with thermally stressed microvias, that are in the process of failure, it is more effective to use a mild microetch. Typically a mild micro-etch is used on microsections to enunciate internal structures within the interconnection. With a mild microetch the crystalline structure of the electrolytic copper, the layers and thickness' of the electroless copper and micro-inclusions within or between copper layers are easily seen. It is necessary, for the effective evaluation of a microvia that is beginning to fail and has only a 10% increase in resistance, to use a mild micro etch for failure analysis. It also must be noted that an aggressive microetch can hide subtle internal structure and create artifacts that could be confused with known defects.

In photos 1 and 2 a good microvia was photographed before and after etching to demonstrate the degree of detail that may be achieved. In photo 2 the layer one foil, electroless copper, interface between the bottom of the microvia and the target pad and the plating on the top of the target pad are easily visualizes after a microetch. In photo 1 all internal detail is not visible. It was demonstrated that a well-controlled micro etch, using hydrogen peroxide and ammonium hydroxide, greatly enhanced the physical details of the failing interconnect and improved the ability to objectively evaluate failures and causative mechanisms. The microvias evaluated in this study had a mild microetch.

### An Un-Etched and Etched Microvia

Photo 1 Before

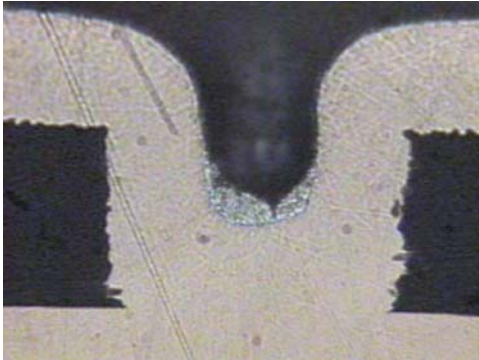
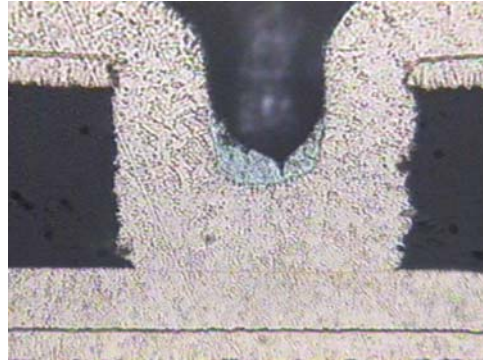


Photo 2 After



### Failure Analysis - Subtle Microvia Failures

IST equipment has the inherent ability to stop testing an individual coupon automatically when it achieves a 10% increase in resistance, in any test circuit. This assures that the failing circuit is stopped before the coupon has achieved a catastrophic failure. Photo 3 is of an obviously failing microvia, while photo 4 has a more subtle failure mode. Both coupons were stopped at a 10% increase in resistance and then identified, with thermal imaging techniques, as the microvias contributing the highest resistance to the failing circuit.

### Microvias Contributing a 10% Increase in Resistance

Photo 3

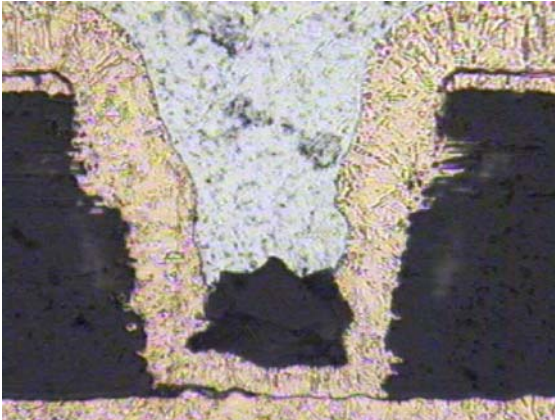
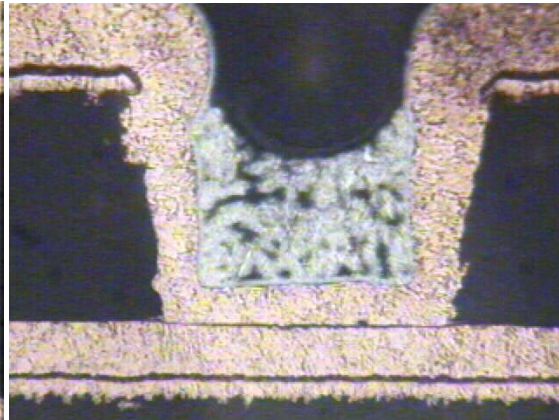


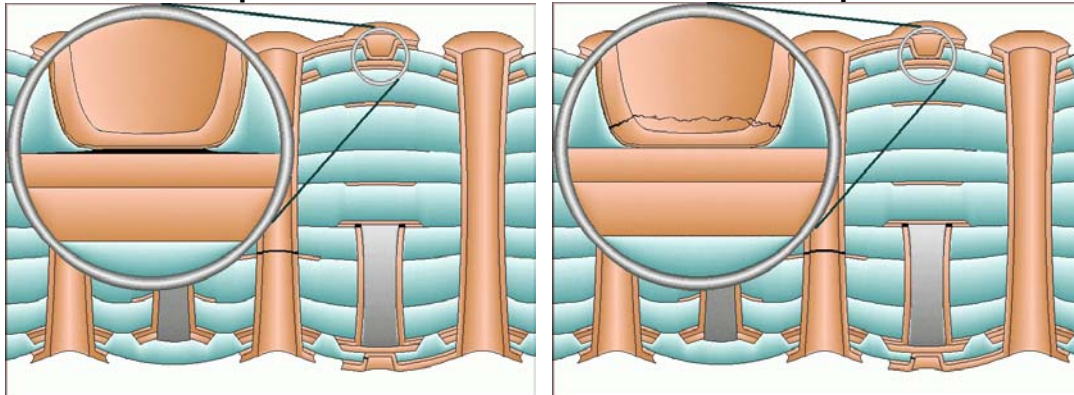
Photo 4



Armed with these tools a comprehensive failure analysis can be achieved. Failure analysis suggested that there were two distinct failure mechanisms at work in these coupons. Barrel cracks were found at the base of the hole wall of a few microvias. Much more common was debris under or above the electroless copper deposit, at the interface with the target pad leading to pad separations. The analysis suggested that the dominant underlying contributor to the microvia

failures in this study was an inherent weakness at the interconnection between the base of the microvia and the target pad. The electroless and electrolytic copper thinned from the knee to the bottom of the microvia and was believed to be a contributing factor to the barrel cracks.

### Two Microvia Failure Modes – Pad Separation and Barrel Cracks



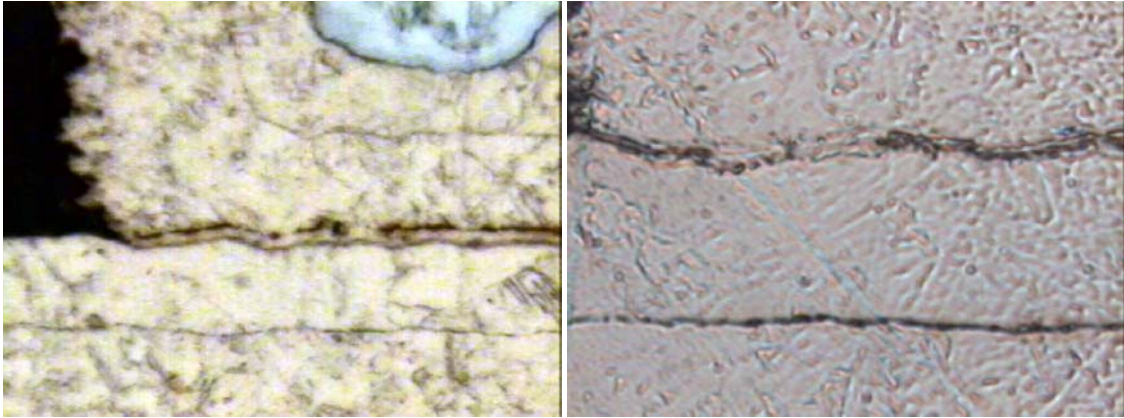
### Common Characteristics of Failing Microvias

After analysis of a large number of failed microvias some common characteristics became apparent. One of the characteristics of failing microvias due to a target pad separation is that they usually exhibited inclusions between the electroless copper and the target pad, or between the electroless and the electrolytic copper. Because we are viewing failing microvias that have not failed completely (fully separated), we have the opportunity to review the failure in progress. The microsection is acting to capture a moment in the time of the failure. We were able to review the most electrically degraded microvia and the neighboring microvias that are in various stages of failing.

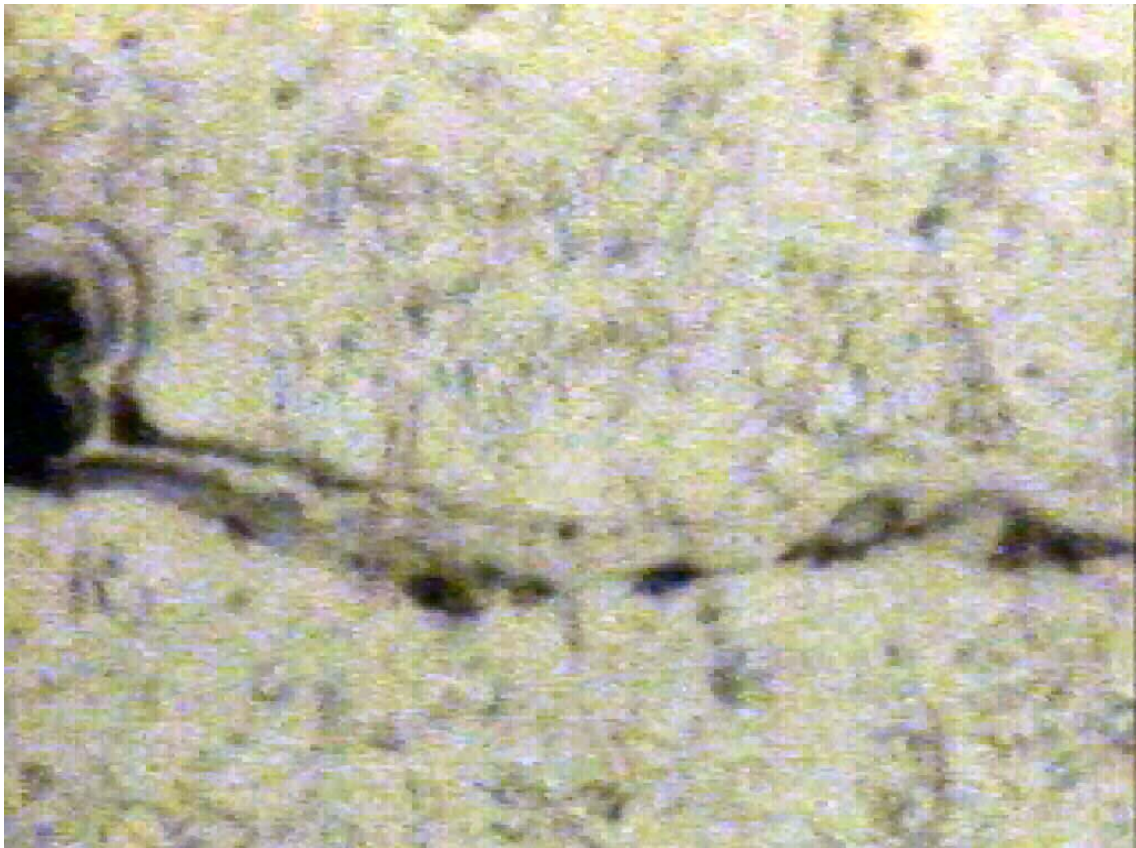
Frequently failing microvias exhibited precursor black dots at the target pad/via plating boundary. The black dots enlarge into small cracks that then coalesce into large cracks. This process is like a tearing along perforations in a piece of paper. Commonly the cracks would appear in the center and at the perimeter at the base of the microvia. Microvias that were advanced in the failing process had the appearance of a crack that started on one side of the base of the microvia and progressed completely across the interface.

Photos 5 and 6 exhibit the precursor black dot above and below the electroless copper. Photo 7 shows coalescing micro-cracks both above and below the electroless copper.

**Precursor “Black Dots” and Coalescing Micro-cracks**  
**Photo 5** **Photo 6**



**Precursor - Inclusions that Coalesce into Cracks – Two Cracks Forming**  
**Photo 7**

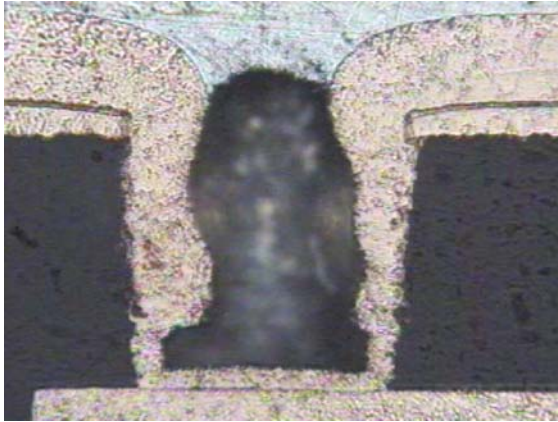




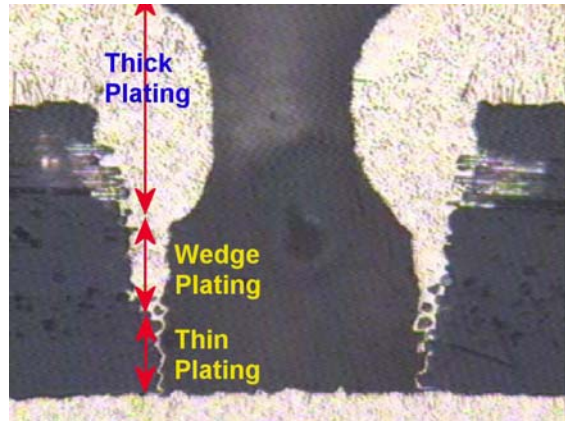
Another observation is that the electroless and electrolytic copper quickly thins below the knee of the microvia. Electroless that measured 120 millionth of an inch on the surface of the pad can be un-measurable at the base of the microvia. The thickness of the electroless and electrolytic coppers was reduced, in some cases dramatically, as the deposit descends into the microvia. The effect of thinning electroless can produce a condition commonly called step plating. Photo 8 demonstrates the reduction in electroless, which is plainly visible on top of the surface foil and only barely discernible at the base of the microvia. Photo 9 is an extreme example of wedge plating on a microvia processed with direct metalization. Usually microvia barrel cracks are associated with process conditions that are rejectable to IPC 6012 or other applicable documents. If these conditions were to be discovered using random microsections the lot would have been rejected. The problem with thinning copper plating is that this condition is random and may occur any where on the board. Not all microvias would have the exact same condition. With failure location method it is very successful in finding this condition when it is random in nature.

**Thinning of Electrolytic & Electroless Copper Below the Knee of the Hole**

**Photo 8**



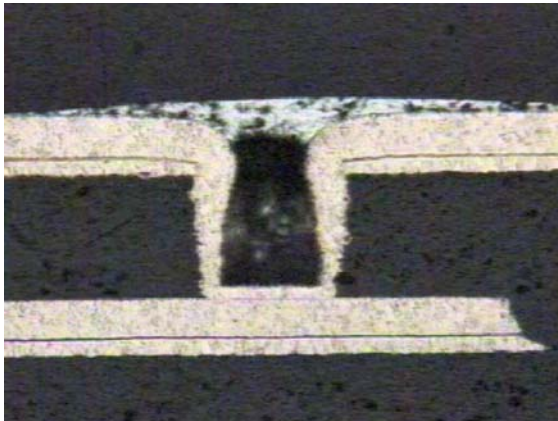
**Photo 9**



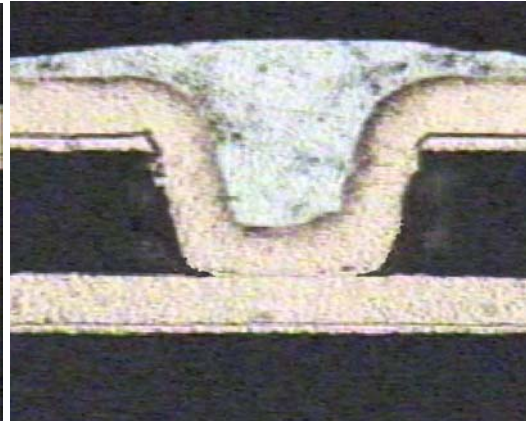
It was found that the shape of the microvia was also contributing to the robustness of a microvias. Bowl shaped microvias appeared to have a more uniform copper distribution to the base, as compared to microvias are cylinder shaped. Bowl shaped microvia were found to achieve higher cycles to failure than cylindrical microvias.

### **Cylindrical Microvia vs. Dish Shaped Microvia**

**Photo 10**



**Photo 11**



Armed with improved microsection techniques and a better understanding of the failure modes Coretec investigated methods of improving microvia fabrication and improved reliability.

### **Coretec Concerns and Considerations**

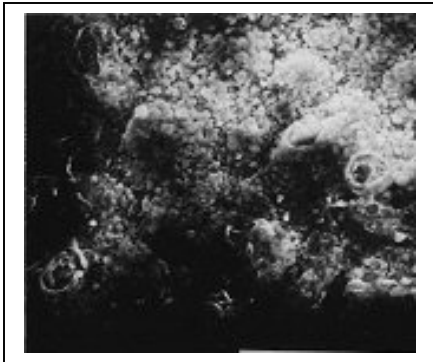
The majority of microvia production within North America is achieved through laser ablation. Two common laser sources are UV and CO<sub>2</sub> laser. These can be used individually, but over the last 5 yrs the employment of hybrid laser has increased. Hybrid laser are dual laser source machines, where the UV laser source would ablate the copper on layer 1 (or n) and the CO<sub>2</sub> laser source would ablate the glass and epoxy dielectric. The CO<sub>2</sub> will not ablate the copper.

The wavelength of the CO<sub>2</sub> laser is 9.8 um. Copper is reflective to the 9.8 um CO<sub>2</sub> emission. The reflected beam will cancel the incoming beam due to a 180-degree phase loss caused by the reflection. This canceling effect will result in a non-absorption zone very close to the reflective copper surface. The actual depth of this non-absorption zone varies depending on the condition of the copper surface and the absorption coefficient of the resin. For rough estimation, the non-absorption zone should be thinner than 1/8 of the wavelength, which is 1.2 um, or 0.000050". In other words, a very thin layer of epoxy will remain on the target pad after CO<sub>2</sub> ablation. The existence of this thin epoxy requires an effective process to clean the copper target pads before they can be plated/metalized. This is accomplished through a KMNO<sub>4</sub> desmear or plasma process.

If the thin resin layer is not effectively removed, surface of the copper target pad will not readily accept copper. This, in most cases, will be expressed as “blotchy” condition such that areas of the target pad will accept copper, and some areas will not. Electroless copper will cover the thin epoxy layer and following electrolytic copper plating, cosmetically, the via will appear to look acceptable. At final inspection the microvia conductive and pass electrical test.

The following images show the surface topography at the various process stages.

**Photo 12**



**Photo 13**



**Photo 14**

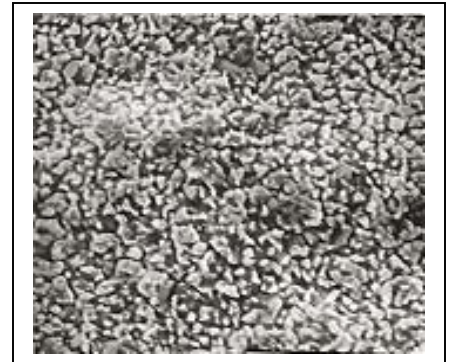


Photo 12: Target pad after laser drilling – Debris is visible

Photo 13: Target plasma desmear and microetch – Some debris remains

Photo 14: Target pad after  $\text{KMNO}_4$  desmear and microetch (no plasma) – Clean

With substandard prepping of the target pad, the final microvia will appear to look and function correctly. During a standard thermal cycle test, the microvia will be reported acceptable. At elevated test temperatures and lead-free assembly parameters, the microvia may fail. The use of IST testing, through Pb free temperature preconditioning, and elevated thermal cycling, sub standard microvia will be identified. This testing will ensure proper process conditions are employed.

### **The Physics of Microvia Failure**

The majority of the strain exerted on a microvia is from the Z-axis expansion of the dielectric. As the dielectric is heated it expands. The coefficient of thermal expansion (CTE) is the change in thickness of the dielectric per degree centigrade. The CTE of dielectric materials used in PWB fabrication are measured in part per million per degree centigrade (ppm/C). Thermal analysis of the FR4 epoxy glass laminate show a CTE that is constant until the glass transition temperature (Tg). At the glass transition temperature the CTE changes, usually increasing by a factor of 3 to 5. A typical CTE of a multilayer PWB is

around 30 ppm/C before Tg and then increase to 150 ppm/C after Tg. Tg is usually found to be between 150<sup>0</sup>C and 180<sup>0</sup>C. At temperatures above Tg the amount of strain exerted on the system is significantly increased.

Because the dielectric is very thin in a microvia, .002" to .004", the amount of strain in the microvia structure is low as compared to a PTH or other interconnect structures. In the typical board construction a microvia is frequently found on the outer layers of the board. The microvia in a typical 16-layer construction is sitting on top of about .070" of dielectric. The CTE of the dielectric below the microvia is the same as the CTE of the dielectric of the microvia structure. Because there is a greater volume of dielectric below the microvia there is a much greater amount of expansion occurring below the microvia. In this study microvias were frequently found to fail in the beginning of the cooling cycle.

Microvias were found that were open at ambient temperatures and then conductive with the application of heat. It appears that an open microvia, one that has a separation from the base to the target pad, may be affected by the expansion or contraction of the material beneath the microvia. If there were microvia to pad separations that occurred during heating, the material below the microvia would drive the target pad into the base of the microvia. The effect was the appearance of a self-healing intermittent open. During the cooling cycle the target pad may be pulled away from the base of the microvia causing either high resistance in the circuit or an open.

It is possible for a failed microvia to act as a thermal sensitive switch that is conductive upon heating then open upon cooling. The microvia may be sensitive to thermal changes or a mechanical deformation typically open without stress. It was found frequently that open circuits, one with failed microvias, could be induced to become conductive with a heating or twisting the board. Under thermal or mechanical strain the circuit would be conductive enough to accept a small current, and thermo graphic techniques would be employed to identify the offending microvia

### **Z-axis Expansion – The Effects of Strain Inside the Microvia Structure**

The main cause of strain on the microvia during thermal excursion is from the Z-axis expansion of the dielectric between the top of the microvia (outer layer) and the capture/target pad. The amount of strain exerted in the microvia structure is in proportion to the thickness of the dielectric. The amount of stress in the system is a function of thickness dielectric, surface area, shear forces and the visco-elastic properties of the dielectric. In this paper we will limit the discussion to strain.

It is obvious that the relatively thin dielectric between the two copper layers of a microvia structure (as compared to the dielectric thickness between

layers 1 and 16 in a PTH), is the major contributing factor to why the “microvia is the strongest interconnect”. There is only .002” to .004” of dielectric to exert strain on the microvia. Microvias are the least stressed electrical interconnection in a typical PWB and therefore considered the strongest interconnection structure.

### Test Temperature Requirements for Microvia Reliability

PWB Inc undertook the study to determine the most effective IST testing parameters for determining if microvias are robust. It was decided that five cycles of preconditioning to 230<sup>0</sup>C required by Curtiss-Wright would be kept as a constant. After preconditioning known discrepant microvia coupons were tested to temperatures of 150<sup>0</sup>C, 170<sup>0</sup>C, 190<sup>0</sup>C, 210<sup>0</sup>C and 220<sup>0</sup>C. The most significant finding was the coupons that were know to be discrepant survived to end of test when tested at 150<sup>0</sup>C. Coupons tested at 170C survived with a mean of 789 thermal cycles to failure. It was not until test temperatures reached 190<sup>0</sup>C were coupons failing below 500 cycles.

**IST Cycles to Failure  
Table 1**

<b>IST Thermal Cycles to Failure – Preconditioned 5 X 230<sup>0</sup>C</b>					
	<b>150<sup>0</sup> C</b>	<b>170<sup>0</sup> C</b>	<b>190<sup>0</sup> C</b>	<b>210<sup>0</sup> C</b>	<b>220<sup>0</sup> C</b>
<b>Mean</b>	1000	789	464	76	44

### Artifacts in the Failure Analysis

Failure analysis of coupons IST tested at 210<sup>0</sup>C or higher revealed failures due to microvia separation but also there were knee cracks, material delamination and breakdown, and barrel cracks. Knee cracks; delamination and material breakdown were considered testing artifacts. It appears that cycle testing at 210<sup>0</sup>C starts the chemical break down of the dielectric. Stress from Z-axis expansion is effectively introduced into the microvia at very high testing temperatures and creates pad separation failures in the same manor as 190<sup>0</sup>C testing, but superimposed on the this failure mode is effects of material failure. CTEs at 210<sup>0</sup>C are so high the materials begin to delaminate, pads experience a significant degree of pad rotation with knee cracks and material darkens as if it were burnt.

Even though the 210<sup>0</sup>C tests easily demonstrated that the microvias were not robust, the presents of artifacts was considered to be an undesirable condition. At 190<sup>0</sup>C the coupons appeared to exhibit the same failure mode as seen in PCBs that failed during assembly.

Based on this data, the IST testing temperature for microvia reliability was raised to 190<sup>0</sup>C (microvia testing only). The cycles to failure of know marginal

coupons were determined to be less than 500 cycles. Testing to 1000 cycles at 190<sup>0</sup>C, IST is capable of differentiating between good and marginal coupons.

**190C Test Protocol Established**

A control test of well made microvias which did not exhibit inclusion, black dots or copper plating concerns where subjected to 1000 IST thermal excursion after 5 X 230<sup>0</sup>C preconditioning. The results were no failures at end of test, 1000 cycles. Robust microvias easily survive 190<sup>0</sup>C testing to 1000 cycles

Based in this data Curtiss-Wright implemented a 190<sup>0</sup>C test protocol for microvias. With the improvements made in fabrication, and the extra advantage of specifying a “high reliability” material, microvias have not been a problem in assembly, rework or in the field.

**The Effect of Lead Free RoHS Assembly and Rework on Marginal Microvia**

An extension of this study was under taken to see the effect of Lead-Free assembly on know marginal microvias. In this part of the study a group of coupons that had known marginal microvias were preconditioned six times at 260<sup>0</sup>C. The first six coupons failed in the first cycle at 190<sup>0</sup>C. It was decided to test this set of coupons at the conservative temperature of 150<sup>0</sup>C in order that we could obtain any qualitative results. The effect of lead-free preconditioning on microvias is profound. The most recent data suggests that the coupons that were able to achieve 788 cycles at 150<sup>0</sup>C were reduced to a mean of 443 after 6 X 230<sup>0</sup>C and 4 cycles after lead free preconditioning of 6 X 260<sup>0</sup>C.

**The Effect of Lead-Free Assembly and Rework On Marginal Microvia  
Table 2**

<b>IST Thermal Cycles to Failure – Various Preconditioning</b>			
	<b>As Received</b>	<b>6 X 230<sup>0</sup> C</b>	<b>6 X 260<sup>0</sup> C</b>
<b>Mean</b>	788	443	4
<b>Minimum</b>	375	204	2
<b>Maximum</b>	925	925	5

Another way to look at this data is to consider the robustness of a coupon in the “as received” state as the coupons entitlement. The entitlement would be the aggregate of the relative quality of fabrication, the material and the board design expressed in thermal cycles to failure. The thermal excursions seen the assembly and rework will cause the degradation of this entitlement. The coupons tested in this part of the study had an entitlement of 788 cycles in the as received condition, or 100%. After precondition at tin-lead temperature (6X 230c to emulate assembly and rework) the entitlement was reduced to 56% and with lead-free assembly emulation the entitlement dropped to 1%. Lead-Free assembly and rework reduced the cycles to failure by 99%.

A group of known good microvia coupons were subjected to “lead-free” preconditioning by exposing them to six cycles to 260<sup>0</sup>C. The samples were then subject to 2000 thermal cycles of 190<sup>0</sup>C. The ‘As Received” coupon achieved a mean of 1923 +/-155 cycles to failure. The preconditioned coupons achieved a mean of 1549 +/- 649 cycles to failure. The reduction in cycles to failure on well-fabricated microvias was only 20% at 2000 thermal cycles.

It appears that RoHS assembly and rework temperatures requirements will be adding enough extra stress that marginal microvias are likely to fail at assembly.

## **Conclusions**

1. Marginal microvias may survive thermal cycle testing below 190<sup>0</sup>C and produce false positive results.
2. Thermal cyclic testing at 190<sup>0</sup>C improves the accuracy of thermal cycle testing and reduces time to results.
3. Failure analysis is improved with microsections that have been subjected a mild micro-etch.
4. Microscopic evaluations of the base of the microvia to pad should include recognition of certain interface characteristic, blacks dots, and micro-inclusion as precursors to compromised microvias.
5. Analysis of the microvia structure should take into consideration the degree that the electroless and electrolytic copper is reduced below the knee of the microvia.
6. Effective and accurate reliability testing requires preconditioning at the appropriate tin/lead or lead-free temperatures for the accurate assessment of microvia robustness.
7. Test temperatures above 190<sup>0</sup>C introduce artifact conditions that may confound failure analysis but still demonstrates relative robustness of microvia structures.
8. The effect of lead –free assembly and rework will break marginal microvia.

## **Acknowledgements**

Appreciation is extended to the management of Curtiss-Wright Controls, Coretec Inc and PWB Interconnect Solutions for the release of IST test results, fabrication considerations and corrective actions in support of this case study. This work was made possible with the equipment and technical knowledge of the personnel at PWB Interconnect Solutions, especially Bill Birch, Neil Copeman, Alex Mendicino and Jason Furlong. Refinements in metallurgical technique were achieved with the support of Flavio Brutesco.

## **Biographies**

Paul Andrews has twenty four years of experience in the telecom, space and aerospace markets in various rolls including test support, manufacturing engineering, mechanical design and quality assurance. Current role Paul is Quality Specialist for PWBs and Final quality Control Manager. He is a Six Sigma Black Belt.

Gareth Parry has over 20 years of experience in the PCB industry, all in senior engineering roles with leading companies such as Hadco, Sanmina and Coretec. Mr. Parry graduated with a Bachelor of Science in Mechanical Engineering from the University of New Brunswick and Manchester University in England. He is a member of the Association of Professional Engineers of Ontario.

Paul Reids' has over 28 years in Engineering and Management Roles in Companies such as Buck-Bee Mears, Printed Circuit Corp., Teradyne Electro Mechanisms, Algorex Inc., RDC Electronique and PWB Interconnect solutions. Mr. Reid received a Bachelor in Science degree in 1975 and a Master in Science in 1980 from Rivier College, Nashua, New Hampshire.

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